EV10AS940-FMC-EVM User Guide

Revision 0.9 – November 2023

If you require any support, please contact your local FAE, or send an email to our hotline at GRE-HOTLINE-BDC@Teledyne.com

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1 Revision History

Table 1: Revision History

Issue	Date	Comments
0.9	November 2023	First version for selected customers

2 Related Documentation

Table 2: Related Documentation

Document type	Number & Issue	Comments
Preliminary datasheet	DS 60S 221987(B)	https://semiconductors.teledyneimaging.com/en/products/data-converters/ev10as940/

3 Introduction

The EV10AS940-FMC-EVM is an evaluation board used to evaluate the EV10AS940 ADC.

The EV10AS940 is a 10-bit Ka-band capable single channel Analog-to-Digital Converter (ADC) allowing a sampling rate up to 12.8GSps. It features Digital Down Conversion (DDC) and Frequency Hopping (FH) capabilities with multiple digital channels thanks to the integration of several NCOs. The EV10AS940 is packaged in an organic substrate to allow high speed and high bandwidth operations.

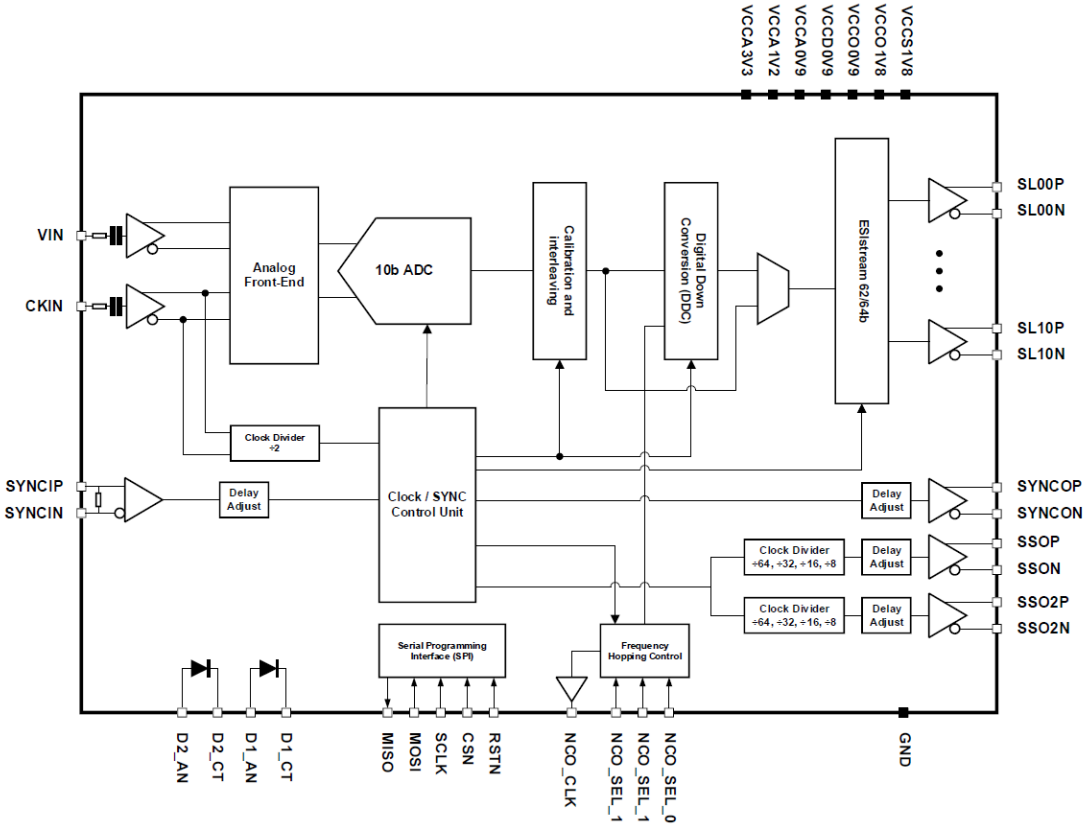

Figure 1: EV10AS940 Block Diagram

4 Hardware Overview

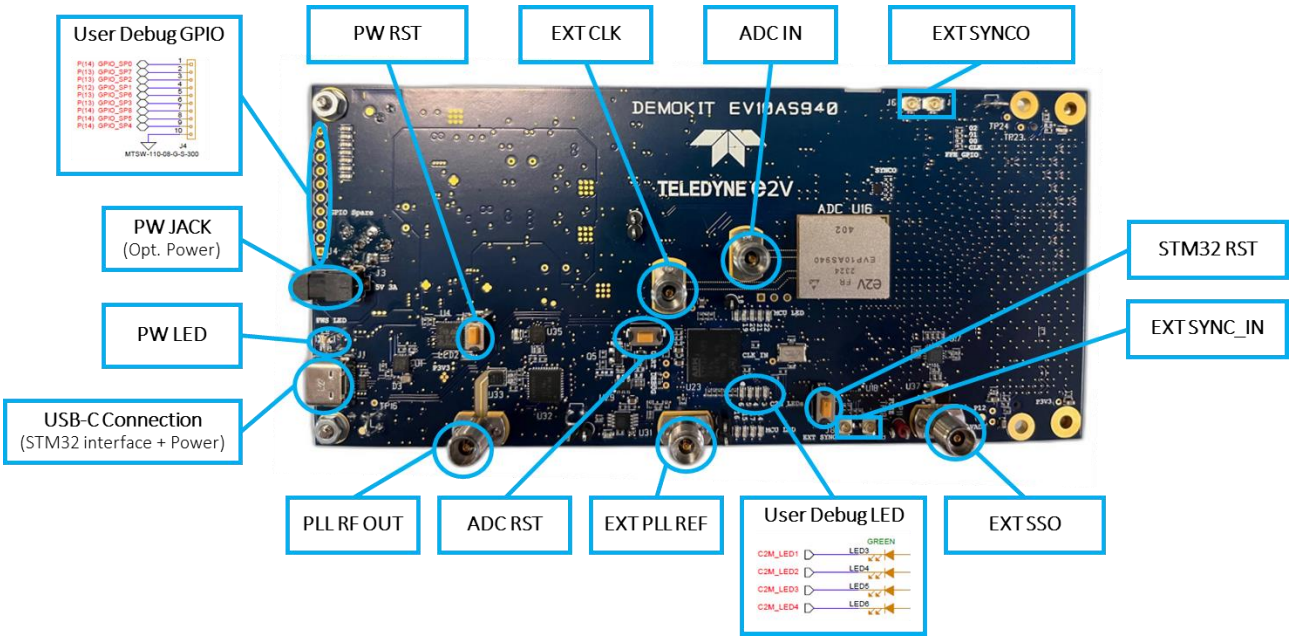

Figure 2: EV10AS940-FMC-EVM top and bottom view

Table 3: Hardware Description

Label	Description	Refer to
USB-C Connection	Connect USB-C cable to computer. Provides power to the board and enables configuration of the ADC and PLL via a GUI.	
PW LED	Indicates whether the USB-C provides sufficient power (5V, 3A).	
PW JACK	Additional power supply in case the USB-C does not provide sufficient power.	
PW RST	Resets all EV10AS940-FMC-EVM power supplies.	
STM32 RST	Resets the STM32.	
ADC RST	Resets the EV10AS940 ADC.	
EXT CLK	ADC clock input. Connect to external signal generator or PLL RF OUT when using the PLL.	6.6
PLL RF OUT	PLL RF output. Connect to EXT CLK when using the PLL.	6.6
EXT PLL REF	PLL external reference clock input. Used to synchronize the board with an external element (e.g a 2nd EV10AS940-FMC-EVM, input or clock signal generator).	6.6
ADC IN	ADC analog input.	
EXT SSO	Optional option to use an external clock for the FPGA high-speed transceiver reference.	6.7
EXT SYNC_IN	External access to the SYNC input of the EV10AS940 ADC.	6.8
EXT SYNCO	External access to the SYNC output of the EV10AS940 ADC.	6.8
User Debug LED	User Debug LED set by the FPGA carrier board	
User Debug GPIO	User Debug GPIO interfacing with the FPGA carrier board	

5 Quick Start

5.1 Hardware and software

The table below lists the FPGA carrier boards validated by Teledyne e2v to support the EV10AS940-FMC-EVM.

Table 4: FPGA Carrier board validated with EV10AS940-FMC-EVM

FPGA FMC+ carrier board reference	FMC+ connector type	VHDL design example	VHDL design example User Guide	Boards assembly
ADA-SDEV-KIT2	FMC+	Contact us	Contact us	

Additionally, ESIstream IP sources are available and can be ported on FPGA evaluation board using these target FPGA.

Table 5: ESIstream IP sources available versus FPGA target

FPGA	ESIstream IP sources	User Guide
AMD/Xilinx Kintex Ultrascale xcku040-ffva1156-2-e	Download sources	Download User Guide
AMD/Xilinx Versal AI Core Series xcv1902-2MSEVSVA2197	Download sources	Download User Guide
Microchip PolarFire MPF300T-1FCG115E2	Download sources	Download User Guide

The EV10AS940-FMC-EVM is compatible with standard FMC+ HPC interfaces. Please contact your local FAE or Teledyne e2v support at GRE-HOTLINE-BDC@Teledyne.com for more information or support on others FMC+ FPGA carrier boards.

5.2 System setup

This early version of the UG assumes a VADJ of 1.8V. In case your FPGA carrier board is not compatible with VADJ at 1.8V, please contact us for guidance.

Complete the following steps to install the EV10AS940-FMC-EVM to a FPGA carrier board. For additional information on FPGA carrier boards, refer to the manufacturer board's user guide.

1. Connect the FPGA carrier board and the EV10AS940-FMC-EVM via the FMC connector,
2. Power-on the FPGA carrier board,
3. Load the FPGA firmware, if necessary,
4. Connect the USB-C cable on the EV10AS940-FMC-EVM,
    a. If the PW LED is green, no additional power is required,
    b. If the PW LED is red, power through the USB-C is insufficient, connect in addition the PW JACK supply,

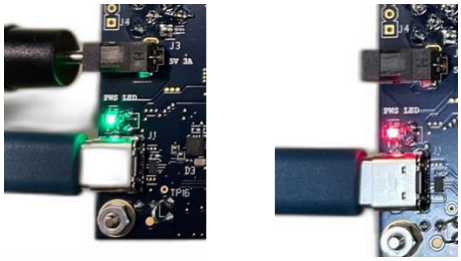

Figure 3: Example of a. PW LED green indicating sufficient power to the board (left) and b. PW LED red indicating insufficient power through the USB-C (right)

5. Connect your external clock signal to EXT CLK SMA connector. If you are using the on-board PLL, connect instead PLL RF OUT SMA connector to EXT CLK SMA connector.
6. Connect your input signal to ADC IN SMA connector,
7. The ADC is ready to be configured and acquire data.

6 Board Technical Description

The EV10AS940-FMC-EVM is a partially populated High Pin Count (HPC) FMC+ mezzanine board.

6.1 Key Features

For the implementation of EV10AS940 ADC, the EV10AS940-FMC-EVM includes the following key features:

- One single-ended input (ADC IN),
- ADC selectable high-speed clock input from the LMX2594 clock synthesizer or from a single-ended clock input (EXT CLK) to evaluate the ADC performance with an external low-noise clock source,
- Selectable internally generated or single-ended input (REF IN) clock reference for the LMX2594 clock synthesizer to synchronize multiple EV10AS940-FMC-EVM boards.
- ADC SYNC selectable inputs from the FMC+ connector or from an external SMA connector (EXT SYNC_IN),
- ADC SYNCO selectable output to the FMC+ connector or to an external SMA connector (EXT SYNCO),
- Selectable high-speed transceiver clock to the FMC+ connector, either the ADC SSO or an external SSO provided through an external SMA connector (EXT SSO),
- Temperature diode monitoring, using LM334 to generate the current source and the integrated ADC of the STM32 microcontroller to measure its voltage,
- 11x High-Speed Speed Lanes (HSSL) to receive ADC samples using ESIstream protocol (see ESIstream protocol specifications).
- Debug user interface, GPIO x9 and leds x4 over FMC+ connector interface,
- STM32 microcontroller and GUI to configure the board and the ADC. The SPI configuration of the board devices can also be managed through the FPGA board and bypass the STM32 and GUI (refer to section 6.5).

6.2 FMC Connector Signals Description

Table 6: FMC Connector Signal Description

FMC+ Pin name	FMC+ Pin Ref	Signal Name	M2C/C2M	Signal Description
CLK0_M2C_P	H4	SSO2P	M2C	Slow Synchro Output (SSOP2 output of ADC). Refer to section 6.7
CLK0_M2C_N	H5	SSO2N	M2C	
CLK1_M2C_P	G2	CLKoutB_P	M2C	PLL RFoutB. Refer to section 6.7
CLK1_M2C_N	G3	CLKoutB_N	M2C	
LA00_P_CC	G6	FH_CLOCK	M2C	NCO_CLK output of the ADC, used for Frequency Hopping hop control
LA01_P_CC	D8	_SPI1_SCLK	M2C	SCLK for SPI1 (STM32 + Carrier Board) interface
LA02_P	H7	_SPI1_MISO	C2M	MISO for SPI1 (STM32 + Carrier Board) interface
LA02_N	H8	_SPI1_MOSI	M2C	MOSI for SPI1 (STM32 + Carrier Board) interface
LA03_N	G10	_CSN_PLLHF	C2M	CSN PLL for SPI2 (STM32 + ADC + PLL + Carrier Board) interface
LA04_P	H10	_CSN_FPGA	M2C	CSN FPGA for SPI1 (STM32 + Carrier Board) interface
LA04_N	H11	_RSTN_FPGA	M2C	RSTN FPGA from STM32
LA05_P	D11	_RSTN_DUT	C2M	RSTN ADC from Carrier Board
LA05_N	D12	FH_GPIO3	C2M	ADC Frequency Hopping hop control GPIO 3
LA06_P	C10	FH_GPIO2	C2M	ADC Frequency Hopping hop control GPIO 2
LA06_N	C11	FH_GPIO1	C2M	ADC Frequency Hopping hop control GPIO 1
LA07_P	H13	SYNC_P	C2M	Synchronization input signal from the FPGA carrier board. Refer to section 6.8
LA07_N	H14	SYNC_N	C2M	
LA08_P	G12	SYNCO_P	M2C	Synchronization input signal from the FPGA carrier board. Refer to section 6.8
LA08_N	G13	SYNCO_N	M2C	
LA09_P	D14	_FPGA_SPI_CTRL	C2M	Set the master of the SPI2 interface between FPGA and STM32. Refer to section 6.4
LA09_N	D15	_PLLHF_SYNC	C2M	PLL SYNC input
LA10_P	C14	_REF_SEL_EXT	C2M	Selection of reference clock for PLL. Set to '1'
LA11_P	H16	_HMC1031_D0	C2M	Set the PLL Feedback division ratio. Refer to section 6.6
LA11_N	H17	_HMC1031_D1	C2M	Set the PLL Feedback division ratio. Refer to section 6.6
LA12_P	G15	_CLKoutB_EN	C2M	Enable PLL RFoutB clock. Refer to section 6.7
LA12_N	G16	_SYNCO_SEL	C2M	Select where the ADC SYNCO is propagated to. Refer to section 6.8
LA13_P	D17	_SYNC_SEL	C2M	Select where the ADC SYNCO is coming from. Refer to section 6.8
LA13_N	D18	_SSO_SEL	C2M	Select which clock signal are propagated to the GBTCLK FMC pins. Refer to section 6.7

FMC+ Pin name	FMC+ Pin Ref	Signal Name	M2C/C2M	Signal Description
LA14_P	C18	_QSPI_IO_DIR_FPGA	M2C	GPIO - STM32 / Carrier Board
LA14_N	C19	_QSPI_IO3	M2C	IO3 of the STM32 QSPI Interface
LA15_P	H19	_QSPI_IO2	M2C	IO2 of the STM32 QSPI Interface
LA15_N	H20	_QSPI_IO1	M2C	IO1 of the STM32 QSPI Interface
LA16_P	G18	_QSPI_IO0	M2C	IO0 of the STM32 QSPI Interface
LA16_N	G19	_QSPI_NCS	M2C	Chip select of the STM32 QSPI Interface
LA17_P_CC	D20	_QSPI_CLK	M2C	Clock of the STM32 QSPI Interface
LA18_P_CC	C22	_SPI2_SCLK	C2M	SCLK for SPI2 (STM32 + ADC + PLL + Carrier Board) interface
LA19_P	H22	_SPI2_MISO	M2C	MISO for SPI2 (STM32 + ADC + PLL + Carrier Board) interface
LA19_N	H23	_SPI2_MOSI	C2M	MOSI for SPI2 (STM32 + ADC + PLL + Carrier Board) interface
LA20_P	G21	_CSN2_PLLHF	M2C	CSN_PLL from STM32 to Carrier Board
LA20_N	G22	_CSN2_DUT	M2C	CSN_DUT from STM32 to Carrier Board
LA21_P	H25	_CSN_DUT	C2M	CSN of ADC for SPI2 (STM32 + ADC + PLL + Carrier Board) interface
LA21_N	H26	_PLLHF_LOCK	CM2C	PLL locked flag. Refer to section 6.6
LA22_P	G24	_PLLHF_EN	CM2C	PLL output enabled. Refer to section 6.6
LA22_N	G25	_GPIO_SPR_MCU0	M2C / C2M	User Debug GPIO 0 - STM32 / Carrier Board
LA23_P	D23	_GPIO_SPR_MCU1	M2C / C2M	User Debug GPIO 1 - STM32 / Carrier Board
LA23_N	D24	_GPIO_SPR_MCU2	M2C / C2M	User Debug GPIO 2 - STM32 / Carrier Board
LA24_P	H28	_GPIO_SPR_MCU3	M2C / C2M	User Debug GPIO 3 - STM32 / Carrier Board
LA24_N	H29	GPIO_SP0	M2C / C2M	User Debug GPIO 0 - Carrier Board / Spare Connector
LA25_P	G27	GPIO_SP1	M2C / C2M	User Debug GPIO 1 - Carrier Board / Spare Connector
LA25_N	G28	GPIO_SP2	M2C / C2M	User Debug GPIO 2 - Carrier Board / Spare Connector
LA26_P	D26	GPIO_SP3	M2C / C2M	User Debug GPIO 3 - Carrier Board / Spare Connector
LA27_P	C26	_C2M_LED1	C2M	Debug User LED 1
LA27_N	C27	_C2M_LED2	C2M	Debug User LED 2
LA28_P	H31	_C2M_LED3	C2M	Debug User LED 3
LA28_N	H32	_C2M_LED4	C2M	Debug User LED 4
HA02_P	K7	_GPIO_SPR_MCU4	M2C / C2M	User Debug GPIO 4 - STM32 / Carrier Board
HA02_N	K8	_GPIO_SPR_MCU5	M2C / C2M	User Debug GPIO 5 - STM32 / Carrier Board
HA03_P	J6	_GPIO_SPR_MCU6	M2C / C2M	User Debug GPIO 6 - STM32 / Carrier Board
HA03_N	J7	_GPIO_SPR_MCU7	M2C / C2M	User Debug GPIO 7 - STM32 / Carrier Board
HA04_P	F7	_GPIO_SPR_MCU8	M2C / C2M	User Debug GPIO 8 - STM32 / Carrier Board

FMC+ Pin name	FMC+ Pin Ref	Signal Name	M2C/C2M	Signal Description
HA04_N	F8	_GPIO_SPR_MCU9	M2C / C2M	User Debug GPIO 9 - STM32 / Carrier Board
HA05_P	E6	GPIO_SP4	M2C / C2M	User Debug GPIO 4 - Carrier Board / Spare Connector
HA05_N	E7	GPIO_SP5	M2C / C2M	User Debug GPIO 5 - Carrier Board / Spare Connector
HA06_P	K10	GPIO_SP6	M2C / C2M	User Debug GPIO 6 - Carrier Board / Spare Connector
HA06_N	K11	GPIO_SP7	M2C / C2M	User Debug GPIO 7 - Carrier Board / Spare Connector
HA07_P	J10	GPIO_SP8	M2C / C2M	User Debug GPIO 8 - Carrier Board / Spare Connector
DP0_M2C_P	C6	SL06-P	M2C	ADC Serial Link 6
DP0_M2C_N	C7	SL06-N	M2C	
DP1_M2C_P	A2	SL10-P	M2C	ADC Serial Link 10
DP1_M2C_N	A3	SL10-N	M2C	
DP2_M2C_P	A6	SL04-P	M2C	ADC Serial Link 4
DP2_M2C_N	A7	SL04-N	M2C	
DP3_M2C_P	A10	SL01-P	M2C	ADC Serial Link 10
DP3_M2C_N	A11	SL01-N	M2C	
DP4_M2C_P	A14	SL05-P	M2C	ADC Serial Link 5
DP4_M2C_N	A15	SL05-N	M2C	
DP5_M2C_P	A18	SL09-P	M2C	ADC Serial Link 9
DP5_M2C_N	A19	SL09-N	M2C	
DP6_M2C_P	B16	SL07-P	M2C	ADC Serial Link 7
DP6_M2C_N	B17	SL07-N	M2C	
DP7_M2C_P	B12	SL03-P	M2C	ADC Serial Link 3
DP7_M2C_N	B13	SL03-N	M2C	
DP8_M2C_P	B8	SL02-P	M2C	ADC Serial Link 2
DP8_M2C_N	B9	SL02-N	M2C	
DP9_M2C_P	B4	SL08-P	M2C	ADC Serial Link 8
DP9_M2C_N	B5	SL08-N	M2C	
DP10_M2C_P	Y10	SL00-P	M2C	ADC Serial Link 0
DP10_M2C_N	Y11	SL00-N	M2C	
GBTCLK0_M2C_P	D4	SSO_P	M2C	Slow Synchro Ouput 1. Can be used as transceiver clock reference by the logic device receiving ADC samples. Refer to section 6.7
GBTCLK0_M2C_N	D5	SSO_N	M2C	
GBTCLK1_M2C_P	B20	SSO2_P	M2C	Slow Synchro Ouput 2. Can be used as transceiver clock reference by the logic device receiving ADC samples. Refer to section 6.7
GBTCLK1_M2C_N	B21	SSO2_N	M2C	
GBTCLK2_M2C_P	L12	SSO3_P	M2C	Slow Synchro Ouput 3. Can be used as transceiver clock reference by the logic device receiving ADC samples. Refer to section 6.7
GBTCLK2_M2C_N	L13	SSO3_N	M2C	

FMC+ Pin name	FMC+ Pin Ref	Signal Name	M2C/C2M	Signal Description
SCL	C30	_SCL	M2C / C2M	I2C Serial Clock. Interface can support Intelligent Platform Management Interface (IPMI) commands
SDA	C31	_SDA	M2C / C2M	I2C Serial Data. Interface can support Intelligent Platform Management Interface (IPMI) commands
GA0	C34	GA0	C2M	Geographical address of the module. Can be used for adressing on I2C bus. Driven by carrier board
GA1	D35	GA1	C2M	Geographical address of the module. Can be used for adressing on I2C bus. Driven by carrier board
PRSNT_M2C_L	H2	PRSNT_M2C_L	M2C	Module present signal. This signal allows the carrier to determine whether an FMC IO mezzanine module is present

M2C = Mezzanine to Carrier Board
C2M = Carrier to Mezzanine Board

6.3 IPMI Identification I2C EEPROM

A Microchip AT24C02C is used as the Intelligent Platform Management Interface (IPMI) EEPROM. This EEPROM provides the EV10AS940-FMC-EVM mezzanine board information to the carrier board for proper voltage settings.

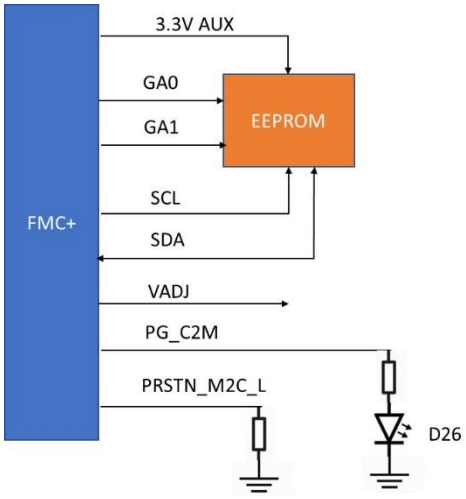

Figure 4: IPMI Identification Interfaces

The procedure is summarized below. Further details on the requirements and protocol for this process are available in the VITA-57 specification.

- The carrier detects the presence of the EV10AS940-FMC-EVM by verifying that PRSTN_M2C_L is asserted low. This happens after the carrier board is connected and powered but before the EV10AS940-FMC-EVM is powered (at that time only the auxiliary 3.3V power rail, 3P3VAUX, is active on the EV10AS940-FMC-EVM),
- Then the voltage requested by EV10AS940-FMC-EVM for VADJ is read from the EEPROM,
    - The EV10AS940-FMC-EVM support 1.8V for VADJ,
- The carrier board will power up the module by applying the requested voltage to VADJ. When the VADJ voltage is valid, the PG_C2M (ie. power good) will be asserted high. This will be visible via LED26 (refer to section 6.9).

The address of the IPMI I2C EEPROM is set through the GA[0:1] signals driven by the carrier board. Refer to Table 7 for the EV10AS940-FMC-EVM EEPROM address.

Table 7: EV10AS940-FMC-EVM EEPROM address

Device Type Identifier				Hardware Slave Address Bits			
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	0	1	0	A2	A1	A0	R/W
1	0	1	0	0 *	GA0	GA1	R/W

** HW connection to GND*

6.4 Board Power Supplies

Table 8 lists the external voltage sources of the EV10AS940-FMC-EVM.

Table 8: External voltage sources

Label	Voltage	Current	Description
Supplied through FMC+ connector			
3P3VAUX	3.3V		Used for IPMI Identification prior to module power-up. Refer to section 6.3.
3P3V	3.3V		Unused
VADJ	1.8V		FMC carrier adjustable I/O voltage supply
Supplied through external connector			
5V_USB	5V	3A	Provided through the USB-C connector. Supplies power to the board through regulators
5V_JACK	5V	3A	Provided through the JACK connector. Supplies power to the board through regulators

In case the USB-C connection and PC are compatible with the USB 3.1 (USB Power Delivery) and able to supply 5V/3A, the jack connection is not needed.

LED1 indicates whether the USB-C connection is sufficient (green) or the additional jack power connection is needed (red). Refer to sections 5.2 and 6.9.Status LED

6.5 SPI Architecture

Two SPI interfaces SPI1 and SPI2 are implemented on the FMC board:

- SPI1 implements an SPI interface between the STM32 MCU and the FPGA Carrier board, where the STM32 MCU is the master. This SPI1 interface is used to support the reference solution with the FPGA Carrier board listed in Table 4. This works alongside the QSPI interface between the STM32 MCU and the FPGA Carrier board to transfer the sample data back to the STM32 MCU and GUI for the reference solution.
- SPI2 implements an SPI interface where either the STM32 MCU or the FPGA Carrier board can be set as master, while the EV10AS940 ADC and the on-board PLL are slaves. Figure 5 illustrates this interface.

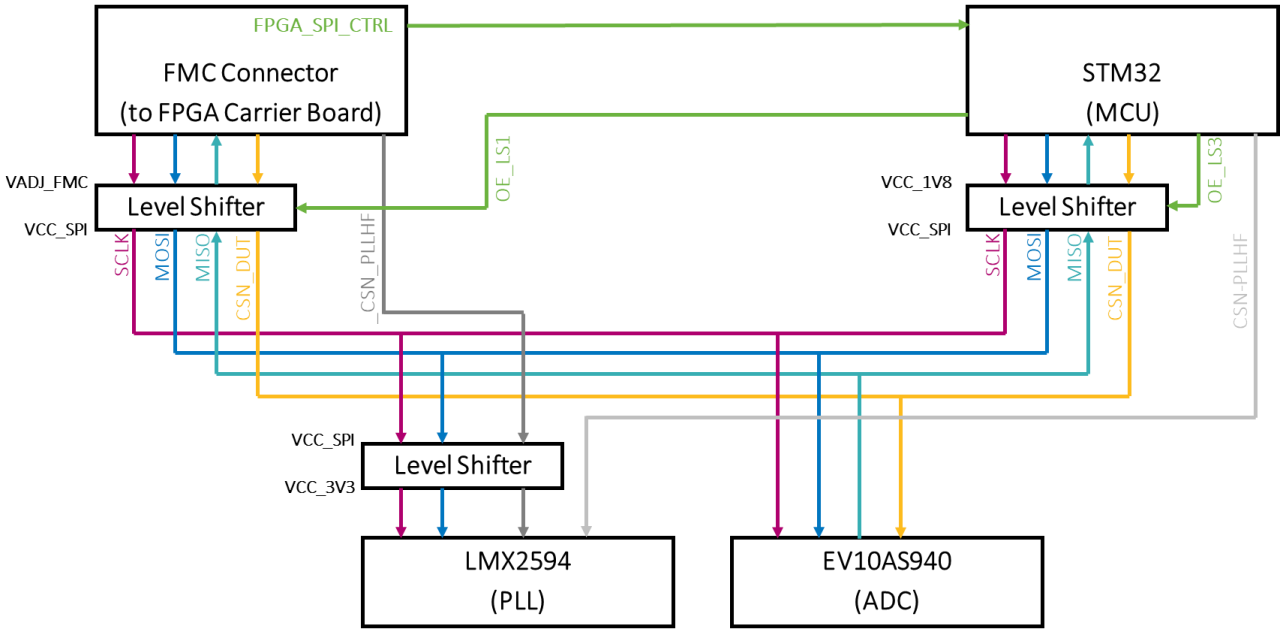

Figure 5: SPI2 Architecture

To select which is the master between the STM32 and the FPGA on the SPI2 interface, the FPGA_SPI_CTRL generated from the FPGA carrier board is used. This signal is received by the STM32 which then sets the enable of the relevant level shifter.

- '0' - The STM32 is the master of the SPI2 bus and can configure ADC and PLL directly,
- '1' – The FPGA is the master of the SPI2 bus and can configure ADC and PLL directly.

6.6 ADC Clock Signals

Two different configurations are possible to feed the ADC input clock.

- Case 1: External clock, the clock is generated by a signal generator and fed to the board and ADC.
- Case 2: Internal clock / External reference, the ADC clock is generated through the onboard PLL with an external reference clock. This option can be useful to synchronize the EV10AS940-FMC-EVM with the rest of the system (e.g other EV10AS940-EVM-FMC boards, the analog input signals).

Figure 6 illustrates the different clock circuit involved in the provision of the ADC clock as well as the related configuration signals. Table 9 shows details on how to configure the PLL feedback division ratio depending on the external reference clock frequency.

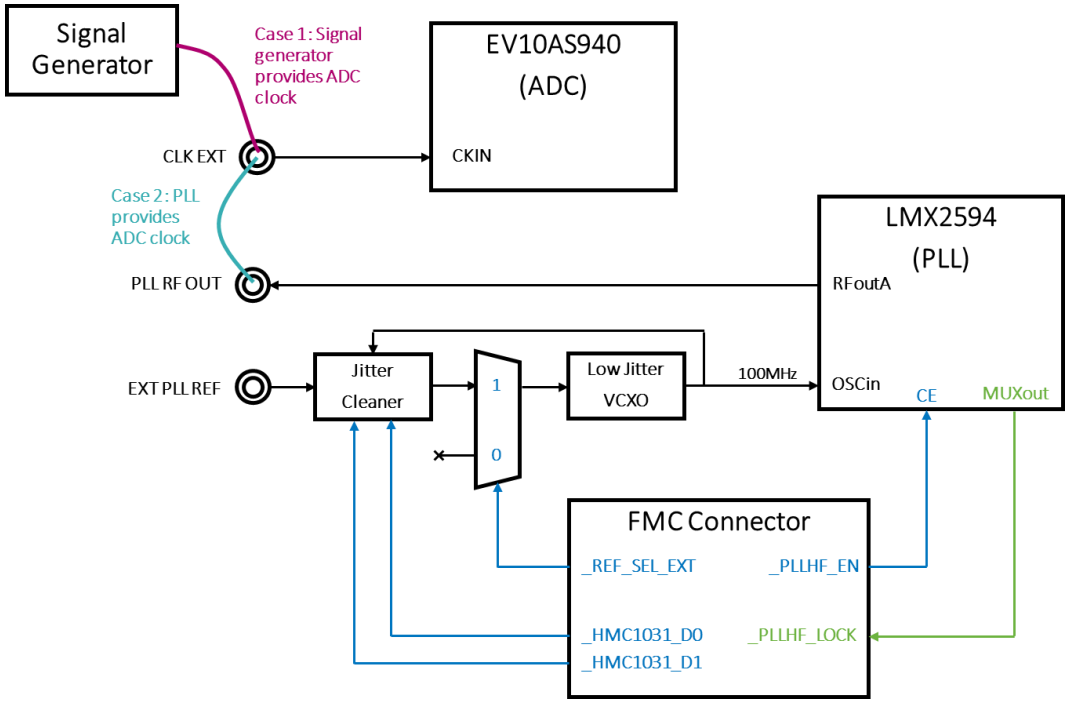

Figure 6: ADC clock signal configuration

Table 9: HMC1031 Configuration Options

EXT PLL REF Frequency	D0	D1	PLL Feedback division ratio
NA	0	0	Power-down
100 MHz	1	0	Divide by 1
20 MHz	0	1	Divide by 5
10 MHz	1	1	Divide by 10

6.7 FMC Clock Signals

Multiple clocks signals are fed from the EV10AS940-FMC-EVM board to the FPGA carrier board through the FMC. Figure 7 illustrates the different clock source and destination as well as the related configuration signals.

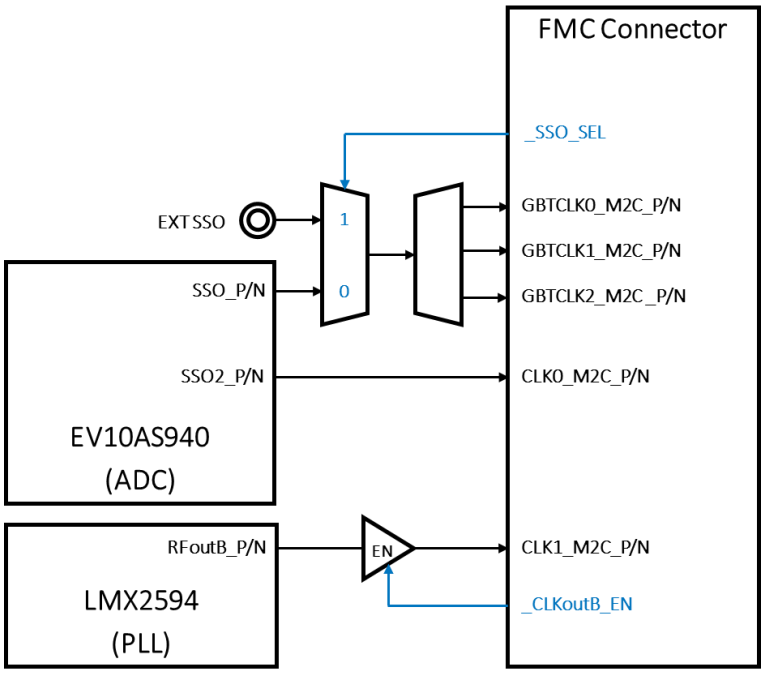

Figure 7: FMC clock signals configuration

6.8 ADC Synchronization Signals

The input and output synchronization signals of the EV10AS940 ADC, can be routed either to and from the FPGA or to and from external connectors. This enables to have either full control of the synchronization signal in the FPGA carrier board or have external access to synchronize the EV10AS940-FMC-EVM to other elements in the system (e.g other EV10AS940-FMC-EVM, signal generator, ...). Figure 8 illustrates the different synchronization signals as well as the related configuration signals.

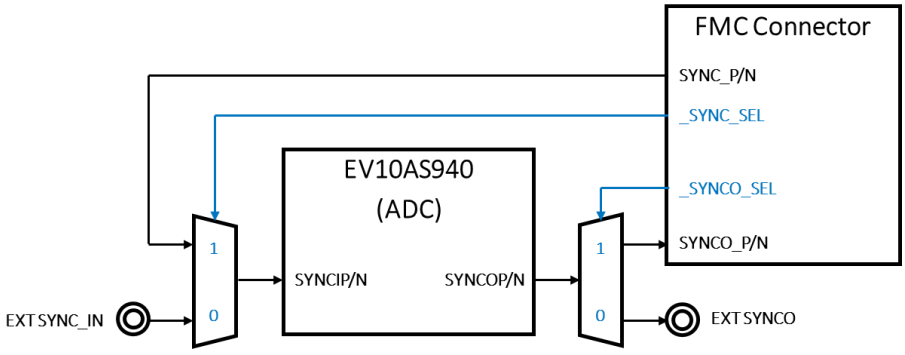

Figure 8: ADC synchronization signals configuration

6.9 Status LED

A number of LED provide status information on the board. Table 10 lists the information they provide. You can refer to drawing top view of the board in annex to locate them.

Table 10: Status LED

LED Label	Type	Status Information
LED1	Power Control	PW LED. If green, USB-C power is sufficient. If red, jack power is required. Refer to section 5.2
LED2	MCU State	Indicate status of MCU. Should be on.
LED3	User Debug LED	User debug LED driven by the FPGA carrier board. Driven low to turn the LED on.
LED4	User Debug LED	User debug LED driven by the FPGA carrier board. Driven low to turn the LED on.
LED5	User Debug LED	User debug LED driven by the FPGA carrier board. Driven low to turn the LED on.
LED6	User Debug LED	User debug LED driven by the FPGA carrier board. Driven low to turn the LED on.
LED7	Power Supply LEDs	Indicates status of VCC 1.8V power supply. Should be on.
LED8	Power Supply LEDs	Indicates status of VCC 3.3V power supply. Should be on.
LED9	Power Supply LEDs	Indicates status of VCCA 3.3V power supply. Should be on.
LED10	Power Supply LEDs	Indicates status of VCCO 0.9V power supply. Should be on.
LED11	Power Supply LEDs	Indicates status of VCCA 1.2V power supply. Should be on.
LED12	Power Supply LEDs	Indicates status of VCCA 0.9V power supply. Should be on.
LED13	Power Supply LEDs	Indicates status of VCCD 0.9V power supply. Should be on.
LED22	MCU State	Indicate state of MCU. Should be blinking when the MCU firmware is running.
LED23	PLL State	Indicates that the external reference clock for the PLL is selected (_REF_SEL_EXT = ‘1’). Should be on when using the PLL to generate the ADC clock. Refer to section 6.6.
LED25	PLL State	Indicates that PLL is locked. Should be on when using the PLL to generate the ADC clock.
LED26	VADJ State	Indicates status of VADJ. Should be on.

7 Graphical User Interface

To be completed for the release version of the UG.

8 ANNEX – EV10AS940-FMC-EVM Drawing

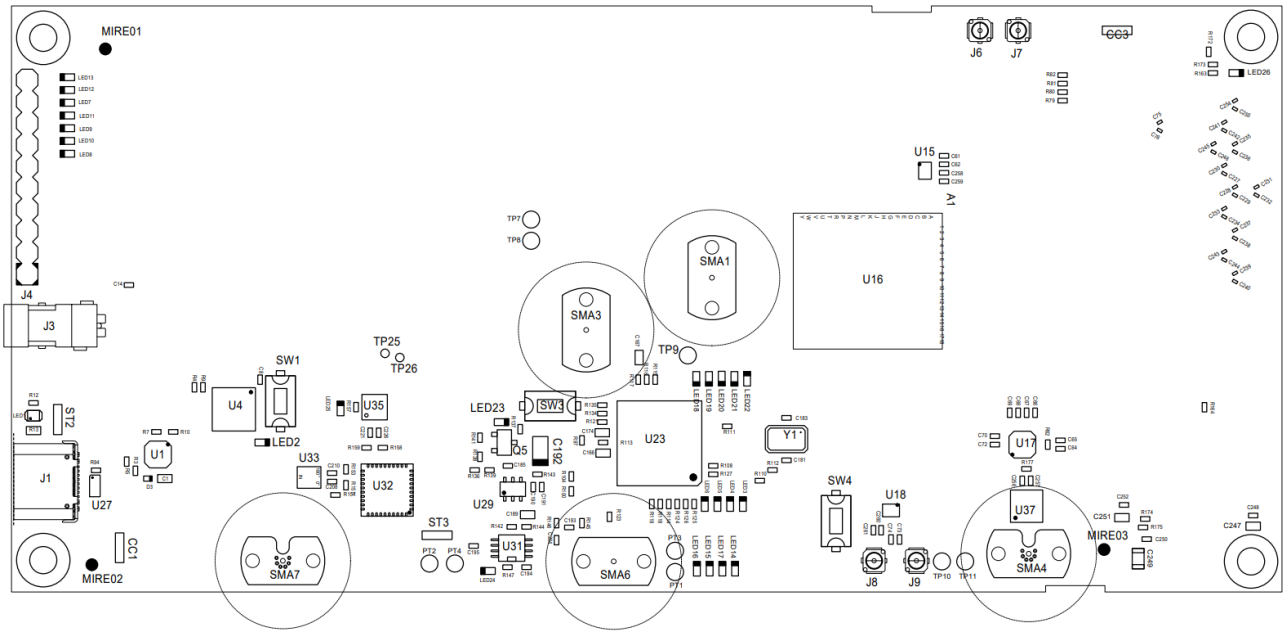

Figure 9: Drawing Top

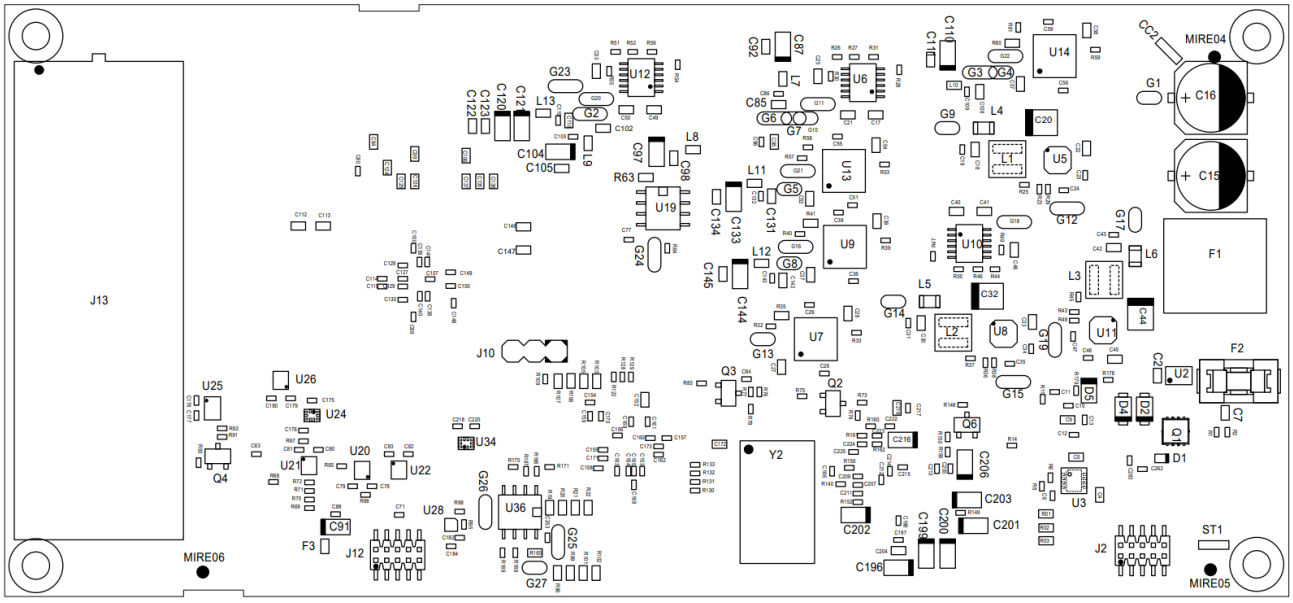

Figure 10: Drawing Bottom

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Mailing Address: Teledyne e2v Semiconductors SAS, Avenue de Rochepleine, 38120 Saint Egrève, France.
Telephone: +33 4 76 58 30 00
e-mail: gre-hotline-bdc@teledyne.com